LOW-POWER BUS INTERFACE

ABSTRACT OF THE DISCLOSURE

A system is configured to disable the bus interface of target devices during periods of inactivity on a bus. A bus controller processes data and control signals from an initiator to establish an initiator-to-target communications path for data-transfer to or from the initiator. At the same time that the bus controller is processing the data and control signals, an activity detector notes the occurrence of the request from the initiator, and enables the bus interface on each of the targets. When the target signals a completion of the data-transfer operation, the activity detector notes the occurrence of the completion signal from target and disables the target interfaces of each target. To provide a substantial reduction in power consumption, the enabling and disabling of the target interfaces is effected by controlling the propagation of the clock system clock to each target interface. The single activity detector is continually active, to detect each data-transfer initiation as it occurs, and effectively eliminates the need for each of the individual target bus interfaces to perform this continual monitoring function.